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Analytic Approach to the Operation of RTD Ternary Inverters Based on MML

Juan Núñez, José M. Quintana & María J. Avedillo
Microelectronics Institute of Seville (IMSE-CNM-CSIC) and University de Seville
Spain

1. Introduction

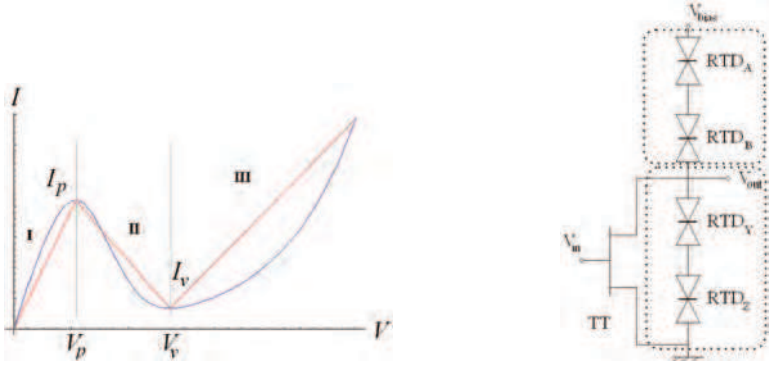
Resonant tunnelling diodes (RTDs) are very fast non linear circuit elements which have been integrated with transistors to create novel quantum devices and circuits. They are today considered the most mature type of quantum-effect devices, already operating at room temperature, and being promising candidates for future nanoscale integration. The incorporation of tunnel diodes into transistor technologies has demonstrated improved circuit performance: higher circuit speed, reduced component count, and/or lowered power consumption (Mazumder et al., 1998), (Broekaert et al., 1998; Sano et al., 2001; Kawano et al., 2003). Thus, RTD based circuits has been receiving a great amount of interest in the last years. Most of the reported working circuits have been fabricated in III/V materials while Si-based tunnelling diodes compatible to standard CMOS fabs are currently an area of active research (Sudirgo et al., 2004). In fact, it has been claimed that augmenting CMOS with RTDs could be the way to extend the lifetime of CMOS and fully exploiting its huge economical investments (Sudirgo et al., 2004). Recent advances in the development of those Si-based RTDs have raised a renewed interest on circuit design using RTDs and transistors.

RTDs exhibit a negative differential resistance (NDR) region in their current-voltage characteristics. Figure 1*a* shows it enhancing key parameters for circuit design: peak current and voltage, I_p and V_p, and valley current and voltage, I_v and V_v. Three regions are defined according to Figure 1*a*: two regions of positive (I and III) and one of negative (II) differential resistance. Circuit applications of RTDs are mainly based on the MOnostable-BIstable Logic Element (MOBILE) (Maezawa & Mizutani, 1993; Akeyoshi et al., 1993; Chen et al., 1995; Pacha et al., 2000; Avedillo et al., 2006a). The basic MOBILE is a rising edge triggered current controlled gate which consists of two RTDs (the load and driver RTDs) connected in series and driven by a switching bias voltage (V_{bias}). When connected in series, RTDs provide multiple-peak structures in their *I-V* characteristics, which make it attractive for multiple-valued logic (MVL) (Waho et al. 1996; Soderstrom, Andersson, 1998; Seabaugh et al. 1992). MVL circuit applications are based on the Monostable-to-Multistable transition Logic (MML) (Waho et al., 1998), an extension of the binary MOBILE. Logic operation is based on the sequential switching (in increasing order of peak current values) of the RTDs connected in series, which is produced when the bias voltage rises to an appropriate value. Logic functionality is achieved by embedding an input stage (compound-semiconductor transistors, HEMT or HBT) which modifies, according the applied input signal, the peak current of some of the RTDs. MML

circuits have been mainly applied in communication system, mainly analog to digital converters and multiple-valued quantizers embedded on sigma-delta modulators, where their high-speed performance is expected to be of the most importance for future commercial applications, (Chibashi et al., 2004; Maezawa, 2005; Eguchi, 2005).

Several works have been dedicated to the performance modelling of MOBILE gates (Quintana & Avedillo, 2005; Aoyama et al., 2002; Matsuzaki et al., 2004; Uemura & Mazumder, 2002; Avedillo et al., 2006b; Quintana et al., 2006) from both a simulation and an analytical point of view. However, an analytical approach allows technology independence and reuse. Some of these papers (Aoyama et al., 2002; Matsuzaki et al., 2004; Uemura & Mazumder, 2002) have studied the maximum operating speed of MOBILE gates. In one of them (Aoyama et al., 2002), it is shown that these gates operate properly in a certain frequency range; that is, they exhibit both a minimum operating frequency and a maximum one. The frequency range depends on the gate fan-out. From the design point of view it should be desirable gates without the minimum limit (correct operation from DC up to a maximum frequency). Through extensive simulations, a relationship between RTD areas and transistor size that must be satisfied for a given MOBILE gate, in a specific technology, to operate properly at very low frequencies can be derived. Analytical design constraints for a DC correct operation have been studied in (Quintana & Avedillo, 2005) which allow designing MOBILE gates without minimum operating frequency problems. In addition, one of the most attractive features of MOBILE-based circuits, as it is their self-latching operation (which allows pipelining at the gate level, and thus very high through-output, without any area overhead associated to the addition of the latches), has been shown to be not inherent to the practical circuit topologies employed to implement MOBILE circuits (Avedillo et al., 2006b), and some analytical design guidelines relating circuit parameters have been developed to avoid the problem (Quintana et al., 2006).

Successful operation of MML circuits has been demonstrated in (Waho et al., 1998), where design of MML ternary inverters and literal gates is addressed. However, an analysis of the self-latching capabilities of the MML structure depending on technological parameters has not



(*a*) (*b*)

Fig. 1. (*a*) I-V characteristic for a LOCOM RTD (blue) and its linear approach (red) and (*b*) typical structure of a MML ternary inverter.

been yet performed. This analysis is crucial to implement quantizers in which the output level must be held even if the input changes (Gan & Su, 1997). To analytically study this problem we have selected a ternary valued inverter and resorted to piecewise linear descriptions for the RTD driving point characteristics, which allow us to obtain relations between RTD and transistor parameters that ensure a correct behaviour of the structure. The chapter is organized as follows: Section II deals with the operation principle of RTD-based ternary inverters. The importance of a correct sizing of the parameters of the structure is analyzed in Section III. The relationships between parameters to ensure a proper behaviour are derived in Section IV, and simulations results using the LOCOM (Prost et al., 2000) technology are shown in Section V. Finally, some conclusions are given in Section VI.

2. Operation Principle

Figure 1b depicts the typical structure of a ternary inverter based on MML composed of four series connected RTDs, one transistor, and driven by a switching bias voltage, V_{bias}). When V_{bias}) rises, RTDs are sequentially switched in increasing order of their peak current values. The high value for the bias voltage is selected in order to have two RTDs switched when it is applied so that three different output voltages can be observed: a low value when the two upper RTDs are switched; a high value when the two RTDs in the bottom are switched and, finally, a medium output value when one of the RTDs in the load and another in the driver are switched. The HFET provides the logic functionality as its input modulates the drain to source current of the transistor, and consequently the effective peak current of some of the RTDs, modifying their switching sequence. In our analysis, we have considered three specific, feasible voltage values of V_{in}, the high (V_{in}^H), medium (V_{in}^M) and low (V_{in}^L) voltages, associated with the logical "2", "1" and "0", respectively.

A first approach to the operation of the structure by analyzing the switching sequence of the RTDs is not suitable to derive relationships among technological and circuit parameters for correct operation, as it is our target, since it is difficult to add the effect of the transistor. This problem can be efficiently solved by considering that two NDR devices can be identified: the load and the driver NDRs (NDR_L and NDR_D, respectively). The first one, the load, is composed of two RTDs (RTD_A and RTD_B in Figure 1b); the second one, the driver NDR, is composed of two RTDs (RTD_Y and RTD_Z) and the transistor TT. The MOBILE operation principle can be applied to this structure consisting of two NDR devices. The order in which transitions are carried out depends on the relationship between the peak currents of each NDR device (Waho et al., 1998).

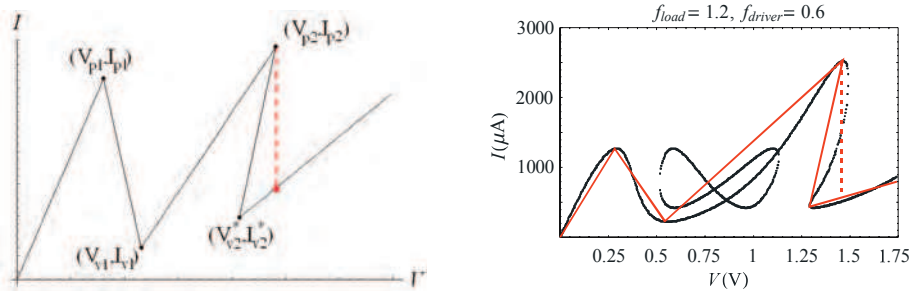
The joint I-V driving point characteristic for two non-linear series-connected RTDs is very complex and some kind of simplification is needed. To perform an analytical study, the I-V characteristic of an RTD has been approximated by a piecewise linear characteristic. Thus, simple geometrical considerations allow obtaining their joint I-V representation. Figure 1a shows this piecewise linear for the RTD obtained from a nonlinear RTD driving point characteristic. Thus, current through the RTD is given by

$$\begin{cases} f\, m_{\mathrm{I}}\, V & V \le V_p \\ f(m_{\mathrm{II}}(V - V_p) + I_p) & V_p \le V \le V_v \\ f(m_{\mathrm{III}}(V - V_v) + I_v) & V \ge V_v \end{cases} \quad (1)$$

where V is the voltage applied to the RTD and f [1] the area factor. If two generic piecewise linear series-connected RTDs, RTD_1 and RTD_2, with area factors f_1 and f_2 respectively ($f_1 > f_2$) are considered, the new joint I-V characteristic has two peak and two valley voltages (V_{p1}, V_{p2}, V_{v1} and V_{v2}, as shown in Figure 2a) which can be easily calculated depending on the values of f_1, f_2, I_p, I_v, V_p and V_v (Gan & Su., 1997). For example, and concerning the peak currents of the new joint IV characteristic, the first one, I_{p1}, is given by the smallest of the individual peak currents ($f_2 I_p$) and the second one, I_{p2}, by the largest one ($f_1 I_p$). The approach is very good as shown in Figure 2b where the driving point characteristic of two non-linear series-connected LOCOM RTDs (with areas $Area_1$=12μm² and $Area_2$=6μm²) and the corresponding joint I-V characteristic from two piecewise linear RTDs which has been theoretically obtained, are depicted. The correspondence between peaks and valleys of both representations becomes apparent.

It is easy to prove that for the representation in Figure 2a, the second valley voltage is always below the second peak voltage. In order to handle well-defined functions, we have made both voltages to be equal and, consequently, the second valley current has been changed as the red dotted line in Figure 2a indicates. The I-V characteristic so obtained does not include some regions that would appear in the complete representation corresponding to two linear series-connected RTDs, but they do not modify the normal operation of the inverter.

The I-V characteristic of both NDR_D and NDR_L shows two peaks and two valleys. Peak and valley voltages and currents in the NDR_L are directly obtained from RTD_A and RTD_B. For



(*a*) (*b*)

Fig. 2. (*a*) I-V characteristic of two series connected RTDs and (*b*) joint I-V representation of two non-linear (in black) and piecewise linear (in red) series-connected RTDs.

NDR_D, peak and valley voltages are directly obtained from RTD_Y and RTD_Z, but peak and valley currents are modified by the transistor, and calculated by adding to the original values (obtained from RTD_Y and RTD_Z) the corresponding amount due to the transistor current for the applied input and a drain to source voltage equal to the peak and valley voltages of the I-V characteristic obtained from RTD_Y and RTD_Z.

Due to the existence of two peaks in the I-V characteristic of both NDR_D and NDR_L, the operation of the ternary inverter shows two "transitions". The relation between the peak currents of the driver and the load during the evaluation phase, depending on the value of the input voltage, will determine the final value of the output voltage (usually RTD areas fulfill the relation $Area_A > Area_B > Area_Y > Area_Z$ (Waho et al., 1998)). For example, if $V_{in}=V_{in}^L$, the relation between peak currents in the NDRs must be $(I_{p1})_D < (I_{p2})_D < (I_{p1})_L < (I_{p2})_L$, where subindex D or L corresponds, respectively, to the driver or the load NDR. In this case, both transitions are due to that RTDs in NDR_D, RTD_Z and RTD_Y are the first to commute and the output is a 'high' level. When $V_{in}=V_{in}^M$, two possibilities can be found to reach a 'medium' logical level of the output: $(I_{p1})_D < (I_{p1})_L < (I_{p2})_D < (I_{p2})_L$ (RTD_Z commutes before RTD_B), or $(I_{p1})_L < (I_{p1})_D < (I_{p2})_L < (I_{p2})_D$ (RTD_B commutes firstly). Finally, for $V_{in}=V_{in}^M$, the relation between peak currents in the NDRs must be $(I_{p1})_L < (I_{p2})_L < (I_{p1})_D < (I_{p2})_D$, i.e., the first and the second transition are due to the RTDs in NDR_L (RTD_B and RTD_A).

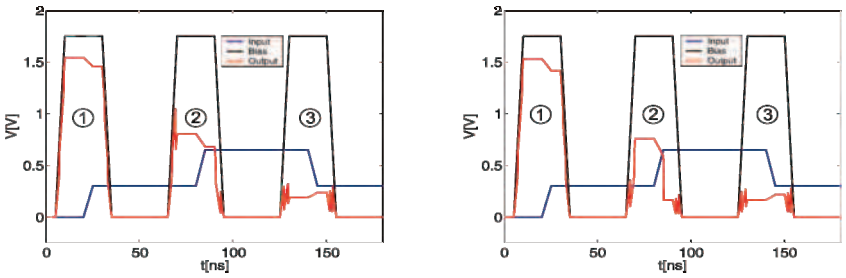
3. The Multistability Disappearance Problem

In order to show concrete examples we have used a piecewise linear model for the RTDs which has been derived from the nonlinear I-V characteristic of RTDs fabricated in the LOCOM (Prost et al., 2000) fabrication process. Figures 3a and 3b show the output response to input voltage changes from two inverters with different sized transistor. Both of them evaluate correctly but, they behave in a different way when the input changes for $V_{bias}=V_{bias}^H$. In the first case (Figure 3a), a variation of the input has no effect on the output, thus, the MML inverter has a correct behaviour. However, for the second inverter (Figure 3b), with a different sized transistor, a change of the input node voltage from V_{in}^M to V_{in}^H forces the output to change from a medium to a low level (multistability disappearance).

A good criterion for predicting this problem can be derived through an analysis of the DC operation of the ternary inverter (Núñez et al., 2006). By applying the Kirchoff Laws to the circuit in Figure 1b, we obtain

$$I_{RTD,L}^{series}[V_{bias} - V_{out}] = I_{RTD,D}^{series}[V_{out}] + I_{DS}[V_{in}, V_{out}] \tag{2}$$

where $I_{RTD}^{series}[v]$ and $I_{DS}[V_{GS},V_{DS}]$ represent the mathematical description of the driving point characteristic of two series connected piecewise linear RTDs ($I_{RTD,D}^{series}[v]$ for the driver and $I_{RTD,L}^{series}[v]$ for the load) and the transistor, respectively. The set of solutions plotted in the V_{in}-V_{out} plane, gives information about what happens when the input voltage changes its value



(*a*) (*b*)

Fig. 3. Input (blue), bias (black) and output (red) voltages for an MML ternary inverter with f_Z=0.6, f_Y=0.7, f_B=1.1, f_A=1.2 and (*a*) W=6μm, L=1μm (does not exhibit multistability problems) and (*b*) W=10, L=1μm (multistability disappearance when the input node changes from $V_{in}{}^M$ to $V_{in}{}^H$).

for a fixed bias voltage. The problem in Figure 3 comes from the disappearance of one (or more) of the stable states in the DC solution representation for V_{bias}=$V_{bias}{}^H$, as it will be explained in the following.

Let us consider the disappearance of the highest output level when the input voltage increases its value to V_{in}=$V_{in}{}^H$ (transition marked as "2" in Figure 3b). This malfunction appears when NDR_L is biased about its first peak voltage (RTD_B is in its peak and commutes, forcing a change in the output node), thus, V_{out} is approximately $V_{bias}{}^H$-$(V_{p1})_L$. Figure 4a depicts the load curve for a properly-sized MML inverter, in which the five solutions found have been marked in red and represented in the V_{in}-V_{out} plane of Figure 4b. Let us consider the case in which the input is fixed at a low value. A malfunction is found around V_{out}≈$(V_{p1})_D$ when V_{in}=$V_{in}{}^L$, which happens when RTD_Z reaches its peak voltage, increasing the value of the output node. In order to find solutions to Eq. (2) around V_{out} ≈ $(V_{p1})_D$ it is mandatory that the first peak current of NDR_D is above the current of NDR_L when it is biased with a voltage equal to $V_{bias}{}^H$-$(V_{p1})_D$ (see Figure 4c and 4d). Finally, if V_{in}=$V_{in}{}^M$, two multistability problems must be analyzed. The first problem, occurs around the maximum value of the output, that is, $V_{bias}{}^H$-$(V_{p1})_L$. To avoid this malfunction, the first peak current of NDR_L has to be above the current of NDR_D when V_{out}= $V_{bias}{}^H$-$(V_{p1})_L$. A similar reasoning is carried out to deal with the malfunction that appears when it is biased with $V_{bias}{}^H$-$(V_{p1})_D$ in which the current through NDR_L has to be under the first peak current of NDR_D.

Let us consider the previously described structures of the MML inverter in figures 3a and 3b. Figure 5a depicts the V_{in}-V_{out} plot corresponding to the one which has the correct behaviour (Figure 3a), where the red dotted line marked with "1" represents the output evolution as V_{in} changes from V_{in}=$V_{in}{}^L$ to V_{in}=$V_{in}{}^M$). The vertical line corresponds to the input medium voltage level and the green point in Figure 5a is the final output value for this transition. The second red dotted line (marked with "2") depicts the output evolution when the input varies from the medium (output marked as a blue point) to the highest level (output as a red point). On the other hand, Figure 5b depicts the V_{in}-V_{out} plot corresponding

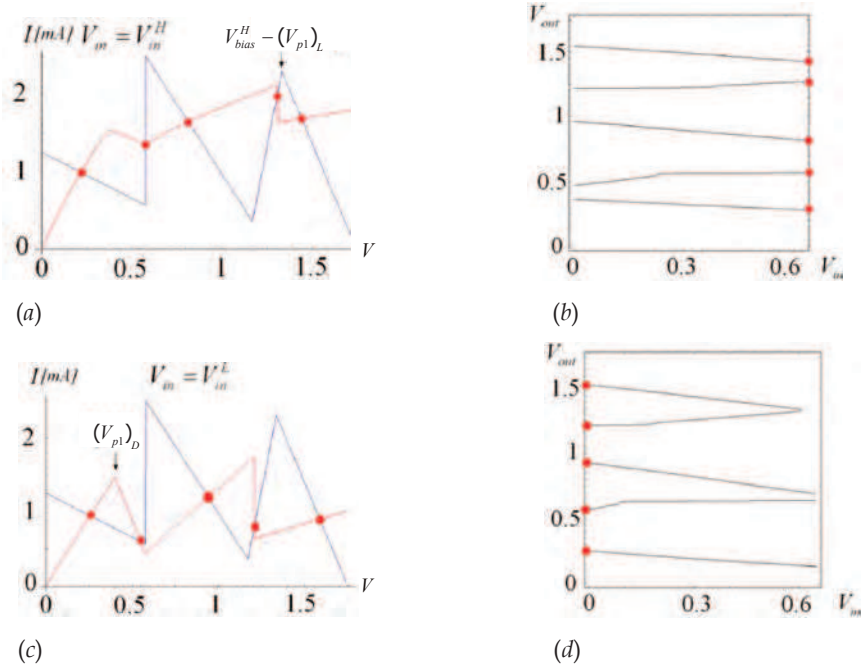


Fig 4. Load curves and V_{in}-V_{out} plots and solutions to Eq. (2) marked in red, for (*a*), (*b*) $V_{in} = V_{in}^{H}$; and (*c*), (*d*) $V_{in} = V_{in}^{L}$.

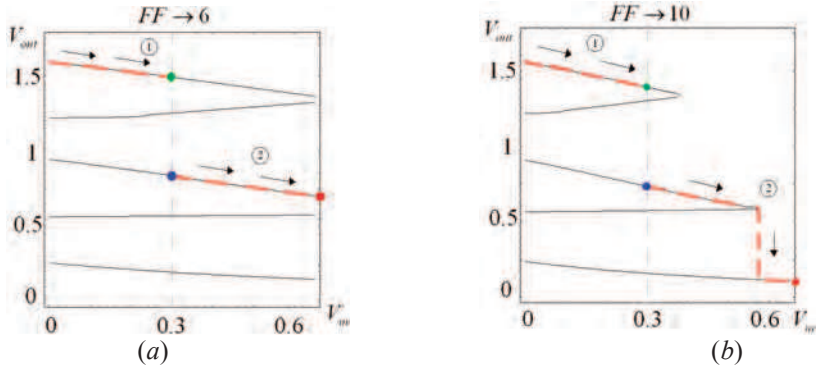


Fig 5. V_{in}-V_{out} plots for the structures of (*a*) Fig. 3*a* and (*b*) Fig. 3*b*, where the red dashed line depicts the evolution of the output as indicated in these figures.

red dotted line marked with "2" (input increasing from V_{in}=V_{in}^{M} to V_{in}=V_{in}^{H}), we can check that when the input voltage is close to 0.6V, the output falls down to the lowest level. The output does not maintain its value and the multistability property is not verified.

4. Critical Dependencies

To guarantee a correct DC operation, we need consider, first, the relations between the area factors of the RTDs and the form factor ($FF = W/L$) of the transistor for a correct evaluation of the structure for fixed input voltages. Case of the transconductance is not proportional to $1/L$ (as in the HFET), this form factor corresponds to W for a fixed L. If V_{in}=V_{in}^{L}, the first transition is due to RTD_Z, thus we must ensure that the first peak current of the driver is less than the first peak current of the load. The critical situation appears when the first peak current of NDR_D is equal to the corresponding one of NDR_L. Thus, the first relation between parameters comes from:

$$f_Z I_p + FF \cdot I_{DS}[V_{in}^{L}, (V_{p_1})_D] < f_B I_p \tag{3}$$

The second RTD to commute is RTD_Y, so that second peak current of the driver must be less than the first peak current of the load (which is originated by the smallest RTD of the load, that is, RTD_B). The limit case is obtained when the first peak current of NDR_L coincides with the second peak current of NDR_D. According to this, a new expression for a maximum value of FF is derived,

$$f_Y I_p + FF \cdot I_{DS}[V_{in}^{L}, (V_{p_2})_D] < f_B I_p \tag{4}$$

Now, if V_{in}=V_{in}^{M}, the sequence of commutation of RTD_Z and RTD_B determines the pair of inequalities to be considered.. Only two of these four inequalities need to be used because they are the most restrictive constraints,

$$f_Y I_p + FF \cdot I_{DS}[V_{in}^{M}, (V_{p_2})_D] > f_B I_p \tag{5}$$

$$f_Z I_p + FF \cdot I_{DS}[V_{in}^{M}, (V_{p_1})_D] < f_A I_p \tag{6}$$

Finally, for the highest input voltage, the RTD switching sequence is RTD_B and then RTD_A, and the following conditions can be derived,

$$f_Z I_p + FF \cdot I_{DS}[V_{in}^{H}, (V_{p_1})_D] > f_B I_p \tag{7}$$

$$f_Z I_p + FF \cdot I_{DS}[V_{in}^H, (V_{p_1})_D] > f_A I_p \tag{8}$$

Four restrictions to the feasible set of values of the circuit parameters can be derived through the analysis performed in Section III. Figure 6a depicts a V_{in}-V_{out} plot for V_{in} increasing from $V_{in}{}^L$ to V_{in}=$V_{in}{}^H$, where the intersections with the right ordinate axis correspond to feasible solutions to Eq. (2) for the high value of the input. Upper point (marked in red) corresponds to a double solution to Eq. (2) and indicates the critical situation for which higher values of *FF* would entail an incorrect behaviour. Thus, an expression concerning to a maximum *FF* is obtained,

$$I_{RTD,D}^{series}[V_{bias}^H - (V_{p_1})_L] + FF \cdot I_{DS}[V_{in}^H, V_{bias}^H - (V_{p_1})_L] < f_B I_p \tag{9}$$

When V_{in} decreases from $V_{in}{}^H$ to $V_{in}{}^L$, the decision is taken around $V_{out} \approx (V_{p1})_D$ (the red point in Figure 6b) and must guarantee that the peak current of the driver is under the current of the load. Thus,

$$f_Z I_p + FF \cdot I_{DS}[V_{in}^L, (V_{p_1})_D] > I_{RTD,L}^{series}[V_{bias}^H - (V_{p_1})_D] \tag{10}$$

For the medium input voltage, V_{in}=$V_{in}{}^M$, two conditions can be derived. A maximum value of FF is obtained by considering that the first peak current of the load must be above the current through the driver (the critical situation is depicted by means of the red point Figure 6c),

$$I_{RTD,D}^{series}[V_{bias}^H - (V_{p_1})_L] + FF \cdot I_{DS}[V_{in}^M, V_{bias}^H - (V_{p_1})_L] < f_B I_p \tag{11}$$

Finally, the last relationship between parameters is derived by considering that the first peak current of NDR_D is equal to the current through NDR_L (as shown in the red point in Figure 6d).

$$f_Z I_p + FF \cdot I_{DS}[V_{in}^M, (V_{p_1})_D] > I_{RTD,L}^{series}[V_{bias}^H - (V_{p_1})_D] \tag{12}$$

5. Simulation Results

In order to check our approach we have performed a comparison between our piecewise linear theoretical approach and HSPICE simulations using the nonlinear RTD model from LOCOM. Eq. 3 to Eq.12 have been employed to analyze how the DC operation of a ternary inverter is modified when some key parameters are changed. HFET and RTDs from the LOCOM technology have been used. For this technology, the RTD has a peak voltage, V_p, of 0.21V, the peak current density is 21 KA/cm² (giving an I_p of 2.1m*A* for an RTD of area factor of 1), and the peak current ratio is about 6.25 at room temperature. The transistor is a depletion HFET with threshold voltage -0.2V. Bias and input levels are $V_{bias}{}^H$=0.175*V*,

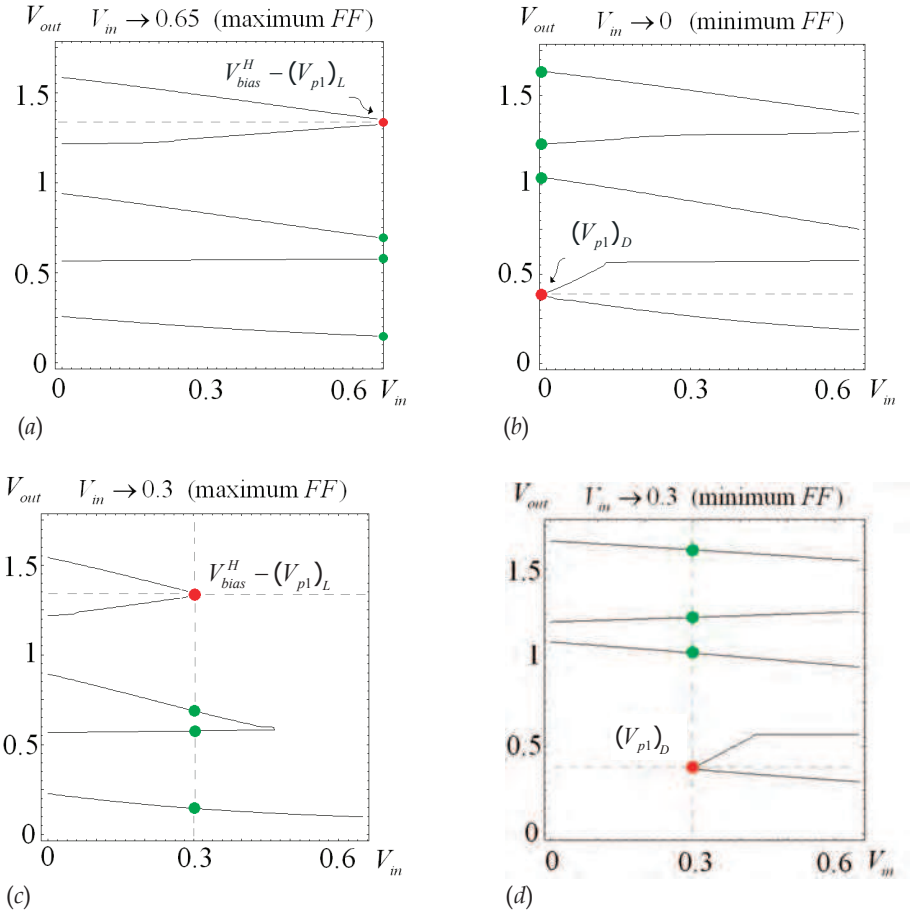


Fig. 6. V_{in}-V_{out} plots pointing out the critical (in red) solutions to Eq. (2) when (*a*) $V_{in} = V_{in}^{H}$, (*b*) $V_{in} = V_{in}^{L}$ and (*c*), (*d*) $V_{in} = V_{in}^{M}$.

V_{bias}^{L}=0V, V_{bias}^{M}=0.3V, and V_{bias}^{H}=0.65V. HSPICE simulations have been performed by using the nonlinear I-V characteristic of individual RTDs.

To reduce the set of parameters which can be modified, we have defined Δ_1 as the difference between the area factors of the RTDs from the same NDR and Δ_2 as the difference between the smallest are factor of the load and the highest of the driver, that is, $\Delta_1=f_Y-f_Z=f_A-f_B$ and $\Delta_2=f_Y-f_B$. Figure 7a shows the set of constraints from which the theoretically correct operation region (the one that guarantees a correct evaluation and multistability preserving operation) can be derived for an inverter with f_Z=0.6 and Δ_1=0.08. Feasible pairs (Δ_2,*FF*) have been calculated by varying Δ_2, as the shady region indicates. Multistability constraint which

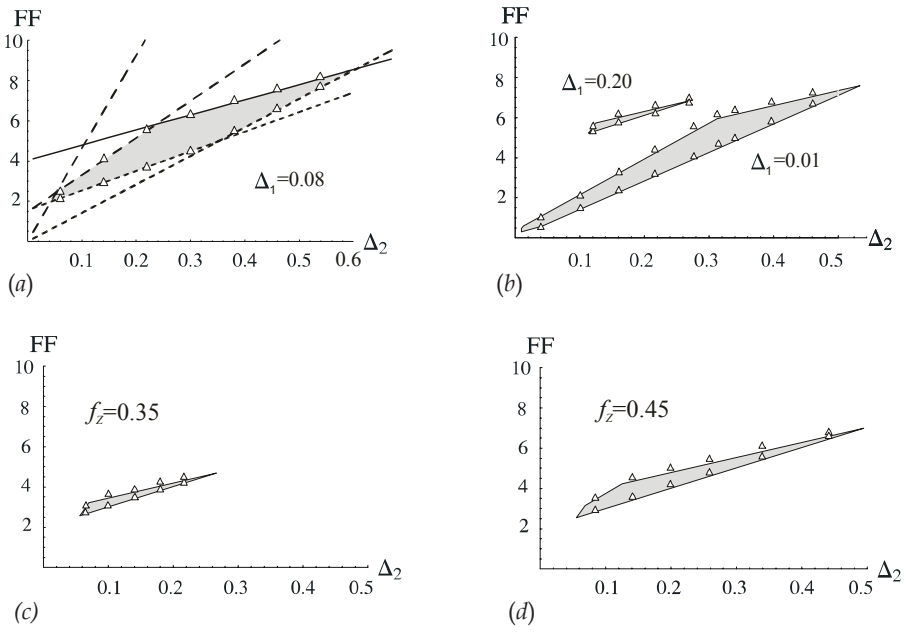


Fig. 7. (*a*) Set of constraints from which the correct operation region is derived. Grey area depicts feasible values of *FF vs.* $\Delta_2 = f_B - f_Y$ for $\Delta_1 = f_A - f_B = f_Y - f_Z = 0.08$ and $f_Z = 0.6$. Triangles delimit the region given by HSPICE simulations with nonlinear RTD models. Feasible (Δ_2,*FF*) pairs for (*b*) $\Delta_1 = 0.01$ and $\Delta_1 = 0.20$, $f_Z = 0.6$. (*c*) $\Delta_1 = 0.1$, $f_Z = 0.35$. (*d*) $\Delta_1 = 0.1$, $f_Z = 0.45$.

provides a maximum FF has been represented by a solid line and evaluation constraints by different broken lines (providing maximum and minimum FF values). From the figure it is apparent the shrinkage of the feasible operation region due to the inclusion of multistability constraints. Figure 7b shows only the feasible sets (the feasible region) for two values of the difference between f_y and f_z (Δ_1), 0.01 and 0.20, respectively. Triangles are operation limit conditions obtained with HSPICE and the nonlinear RTD models from LOCOM. It can be observed the progressive shrinking of the feasible region and the agreement between theoretical and simulation results. Practically, for $\Delta_1 > 0.2$ there are no inverters with a proper behaviour for this value of f_Z. In Figures 7c and 7d the effect of a modification of f_Z is analyzed. A very close correspondence between both theoretical and simulation results can be also observed.

Figure 8a depicts feasible areas of correct operation when $\Delta_1 = \Delta_2 = \Delta$ for different values of f_Z, where the feasible region is widen when f_Z increases its value. Finally Figures 8b and 8c depict pairs (Δ_{1D},*FF*) and (Δ_{1L},*FF*), that allow a correct DC operation, where $\Delta_{1D} = f_Y - f_Z$ and $\Delta_{1L} = f_A - f_B$, (for $\Delta_2 = 0.1$). Small values of Δ_{1L} give narrow regions of correct behaviour, whereas an increase of Δ_{1D} shifts up the feasible area of correct DC operation.

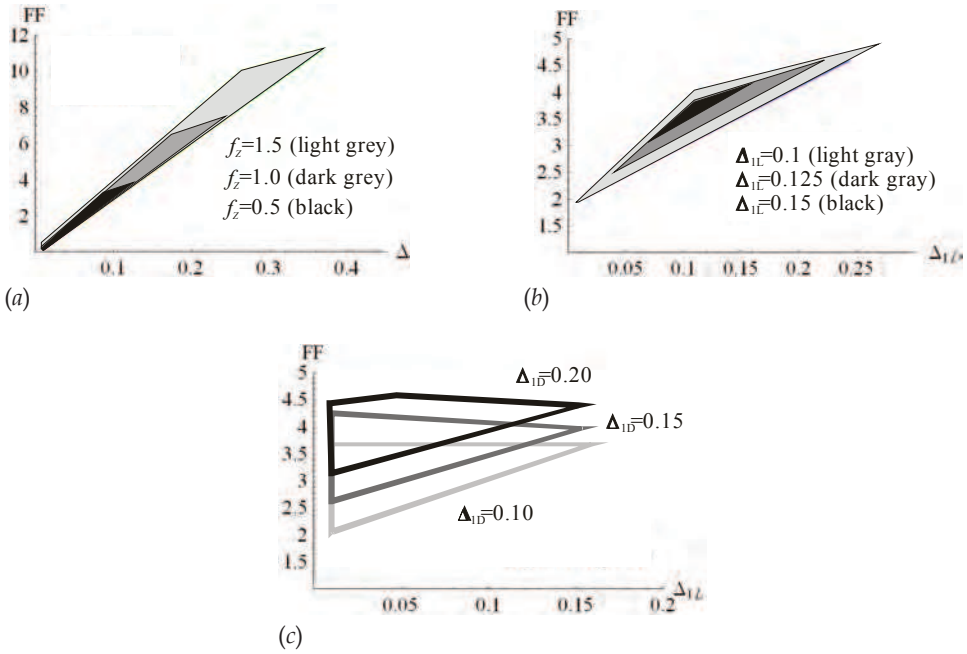


Fig. 8. (*a*) Region of correct DC behaviour *FF* vs $\Delta = \Delta_1 = \Delta_2$ for f_Z={0.5, 1.0, 1.5}. (*b*) *FF vs.* $\Delta_{1D} = f_Y - f_Z$ for $\Delta_{1L} = f_A - f_B$ ={0.1,0.125,0.15} and (*c*) *FF vs.* Δ_{1L} for Δ_{1D}={0.1,0.15,0.20}, with Δ_2=0.1.

The effect of the variation of the peak current density, j_P, is analyzed in Figure 9a by depicting feasible pairs (Δ_2,*FF*) for j_P=18, 42 and 66 KA/cm², and Δ_1=0.01. By increasing j_P, the feasible region is widened and shifts counterclockwise. Finally, Figures 9b and 9c depict the correct operation region for two different values of the peak voltage, V_P=0.24 and V_P=0.15, respectively, and keeping constant the values of the other parameters. A reduction of the final set of feasible pairs (Δ_2,*FF*) is observed while decreasing V_P. HSPICE simulation results have been also included.

6. Conclusions

One additional problem to size the MML inverter used in quantizers has been pointed out. It is the multistability fault, which can prevent the correct operation of circuits, such as quantizers, in which this property is essential. To analytically study the problem, a piecewise linear description for the RTD driving point characteristics has been used. A procedure to calculate the relationships between circuit parameters in order to obtain correct

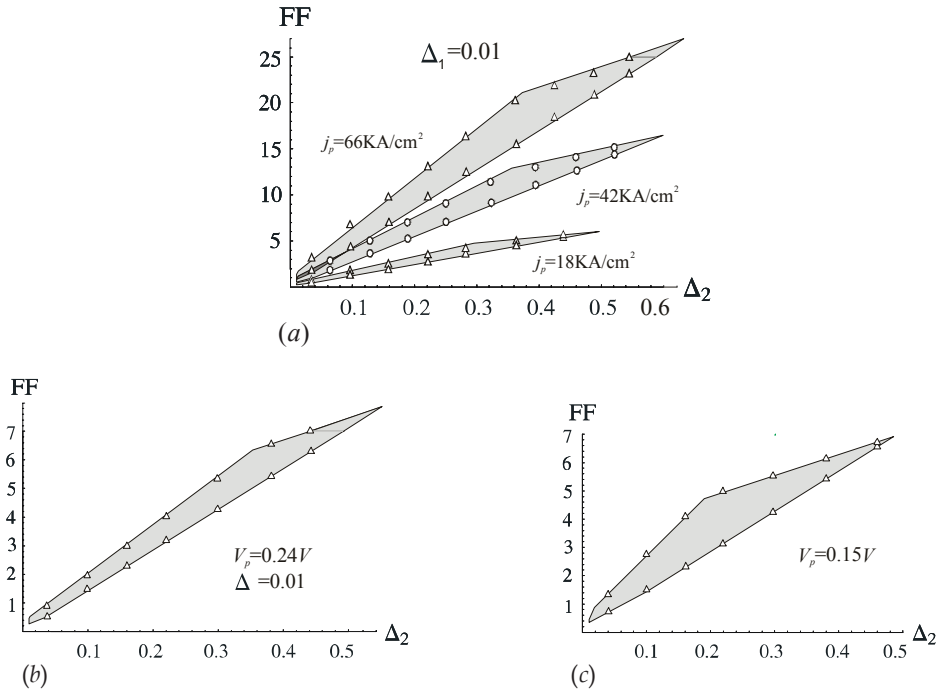


Fig. 9. Set of feasible of values of *FF vs.* $\Delta_2 = f_B - f_Y$ for $\Delta_1 = f_A - f_B = f_Y - f_Z = 0.01$. (*a*) Effect of the variation of j_p. Correct DC operation region for j_p={18, 42, 66}KA/cm². Feasible pairs (Δ_2,*FF*) for different values of the peak voltage, (*b*) V_p=0.24*V* and (*c*) V_p=0.15*V*.

DC operating regions has been derived. HSPICE simulations using a nonlinear RTD model agree very well with our piecewise approach.

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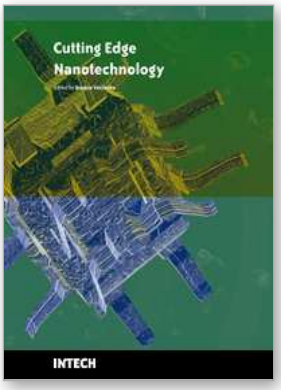

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The main purpose of this book is to describe important issues in various types of devices ranging from conventional transistors (opening chapters of the book) to molecular electronic devices whose fabrication and operation is discussed in the last few chapters of the book. As such, this book can serve as a guide for identifications of important areas of research in micro, nano and molecular electronics. We deeply acknowledge valuable contributions that each of the authors made in writing these excellent chapters.

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University Campus STeP Ri
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Phone: +86-21-62489820
Fax: +86-21-62489821